Course Title

Introduction to digital system design based on FPGA

Students:

Ph.D. students enrolled in the PhD in SCIENCE AND TECHNOLOGY FOR ELECTRONIC AND TELECOMMUNICATION ENGINEERING (STIET)

Duration:

12 hours

Instructor:

Dr. Ali Ibrahim, Assistant Professor

STIET Teaching board

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Course Level

- Basic

Prerequisites and Basic knowledge

- Basic knowledge of hardware description language e.g. VHDL or Verilog
- Basic knowledge of Embedded Systems e.g. Microcontroller and microprocessors architectures.
- Basic Programming skills (C, C++)

Course Description

The course provides an introduction to digital system design using Field Programmable Gate Arrays (FPGA) devices. It starts with a general introduction about the digital system design flow and highlights the importance of the FPGAs in such a system. The course identifies the technologies, architectures, and different components of the FPGA devices. The course provides the students with the required background to get familiar with using CAD tools for the digital system design-based FPGA flow implementation starting from the Register Transfer Level (RTL) design until the configuration on the device. The FPGA implementation flow using high-level synthesis with its application on the design flow is provided. The course includes two in-class practical sessions on the FPGA implementation: the first based on RTL design and the second using High Level Synthesis (HLS) flow.

Course Content

1. **Introduction to Digital system Design**
   1.1. Introduction to Digital System design
   1.2. Introduction to FPGA
   1.3. FPGA design flow
   1.4. FPGA architectures
2. **CAD tools for FPGA based digital system design**
   2.1. Discovering CAD tools e.g. Xilinx Vivado tool and its Flow
3. **RTL Design Example**
   3.1. Implementation from RTL to Binary file generation
   3.2. Synthesis report
   3.3. Power consumption analysis
4. **High Level Synthesis (HLS)**
   4.1. Introduction
   4.2. Design flow
   4.3. Integration with RTL design
5. **HLS Design Example**
   5.1. Implementation from C code to Binary file generation
   5.2. Implementation reports
6. **Case Studies of FPGA Implementations**
   6.1. Projects from the Ph.D. topic

Course Outcomes

After successful completion of the course, students will be able to:

- **Recognizing** the importance of field programmable gate arrays FPGA devices in the design of digital systems.
- **Identifying** the technologies, architecture, and different components of the Xilinx-based FPGA devices.
- **Getting familiar** with the use of the Xilinx Vivado CAD tool for the FPGA flow implementation starting from the RTL design until the configuration on the device.
- **Demonstrating** an understanding of the FPGA implementation flow using high-level synthesis with its application on the design flow.